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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re the Application of		TI-29058
	Mandy Mei-Feng Tsai	Art Unit: 2182
Serial No.:	09/535,226	Examiner: Joshua D. Schneider
Filed:	March 24, 2000	Conf. No.: 2779
For:	Interface Between Different Clock Rate Components	

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at **703-872-9306** on the date shown below:

Robin E. Barnum

April 26, 2004
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FACSIMILE COVER SHEET

X	FACSIMILE COVER SHEET	___	AMENDMENT X (# Pages)
___	NEW APPLICATION	___	EOT (# Page)
___	DECLARATION (# Pages)	___	NOTICE OF APPEAL (# Pages)
___	ASSIGNMENT (# Pages)	X	**APPEAL BRIEF (10 Pages)**
___	FORMAL DRAWINGS	___	ISSUE FEE (# Pages)
___	INFORMAL DRAWINGS	___	REPLY BRIEF (IN TRIPLICATE) (# Pages)
___	CONTINUATION APP'N (# Pages)	X	**Appeal Brief Fee TL (1 page)**
___	DIVISIONAL APP'N		

NAME OF INVENTOR(S): Mandy Mei-Feng Tsai	RECEIPT DATE & SERIAL NO.: **Serial No.: 09/535,226** **Filing Date:** March 24, 2000
TITLE OF INVENTION: Interface Between Different Clock Rate Components	
TI FILE NO.: **TI-29058** / DEPOSIT ACCT. NO.: **20-0668**	
FAXED: 4/26/04 DUE: 4/26/04 ATTY/SEC'Y: RDM/reb	

Texas Instruments Incorporated
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U.S. PATENT AND TRADEMARK OFFICE
APPEAL BRIEF TRANSMITTAL FORM

TI-29058
Docket No.

OFFICIAL

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Robin E. Barnum

In re Application of

Mandy Mei-Feng Tsai

Serial No: 09/535,226

Filed: March 24, 2000

For: Interface Between Different Clock Rate Components

Conf. No: 2779

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an Appeal Brief in the above-identified application.

Please charge the $330.00 fee for filing the Brief to Texas Instruments Incorporated, Deposit Account No. 20-0668.

Charge any additional fees, or credit overpayment to Texas Instruments Incorporated, Deposit Account No. 20-0668.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Tsai
Art Unit: 2182
Serial No.: 09/535,226
Examiner: Joshua D. Schneider
Filed: March 24, 2000
Docket: TI-29058
For: INTERFACE BETWEEN DIFFERENT CLOCK RATE COMPONENTS

Appeal Brief under 37 C.F.R. §1.192

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §1.192 and the Notice of Appeal filed February 24, 2004. This Appeal Brief is timely under 37 C.F.R. §1.7 because April 24, 2004 is a Saturday and the transmission date of this Appeal Brief under 37 C.F.R. §1.6(b) is the next following day that is not a Saturday, Sunday or Federal Holiday.

Real Party in Interest under 36 C.F.R. §1.192(c)(1)

The real party in interest in this application is Texas Instruments Incorporated, a corporation of Delaware with its principle place of business in Dallas, Texas. An assignment to Texas Instruments Incorporated is recorded at reel 013395 and frames 0377 and 0378.

Related Appeals and Interferences under 36 C.F.R. §1.192(c)(2)

There are no appeals or interferences related to this appeal in this application.

Status of the Claims on Appeal under 37 C.F.R. §1.192(c)(3)

Claims 1 to 4 and 11 to 14 are pending and finally rejected. Claims 5 to 10 are canceled.

Status of Amendments Filed After Final Rejection under 37 C.F.R. §1.192(c)(4)

No amendments to the claims were proposed in the response after FINAL REJECTION filed December 18, 2003.

Summary of the Invention under 37 C.F.R. §1.192(c)(5)

This invention is a circuit for interfacing between a first component operating at a first clock rate and a second component operating at a second clock rate where the second clock rate is higher than said first clock rate. The circuit includes a first buffer, a second buffer and a copy/access controller. The first buffer is coupled to the first component. The first buffer receives and stores data from the first component at the first clock rate. The second buffer supplies data to the second component at the second clock rate. The copy/access controller is connected to the first and second buffers to control data movement. The copy/access controller operates to copy data from the first buffer to the second buffer when the first buffer is substantially full. The copy/access controller also prompts the second component to access the second buffer when the data is copied from the first buffer. This invention is also a corresponding method for interfacing the first and second components.

The first buffer and the second buffer may be random-access memories or shift registers.

The circuit may be integrated onto a semiconductor die with one of the first component or the second component.

Statement of Issues Presented for Review under 37 C.F.R. §1.192(c)(6)

Are claims 1 to 4 and 11 to 14 made obvious under 35 U.S.C. 103(a) by the combination of Frankel et al. U.S. Patent 4,463,443 and Kaneko U.S. Patent 5,561,672?

Statement of the Grouping of Claims under 37 C.F.R. §1.192(c)(7)

The Applicants respectfully submit that the claims of this application stand together as a single group.

Arguments

Claims 1 to 4 and 11 to 14 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Frankel et al. U.S. Patent 4,463,443 and Kaneko U.S. Patent 5,561,672.

Claims 1 and 11 recite subject matter not made obvious by the combination of Frankel et al and Kaneko. Claim 1 recites a copy/access controller "operable to copy data from said first buffer to said second buffer when said first buffer is substantially full." Claim 11 similarly recites the step of "copying data from said first buffer to a second buffer operable at said second clock rate when said first buffer is substantially full." These limitations define conditions upon which data stored in the first buffer is copied to the second buffer. These limitations are not made obvious by the combination of Frankel et al and Kaneko.

The FINAL REJECTION cites elements 10 and 18 of Figure 1 of Frankel et al described at column 1, lines 61 to 65 and making

obvious the claimed first buffer. Frankel et al states at column 1, lines 61 to 65:

> "The present invention utilizes a random access memory (RAM) for data storage of data that has clocked into an input register synchronously with an input clock. The data is then transferred to a RAM input holding register, and finally into the RAM."

The Applicant respectfully submits that this portion of Frankel et al includes no teaching regarding the "substantially" full limitation of claims 1 and 11. Frankel et al states at column 3, lines 51 to 57:

> "The data enters the buffer at the input data register 10 synchronously with the input data clock and is transferred to the RAM input register 18 when the input data register 10 is full. The transfer enables the next sequence of RAM write signals from the write/read sequence generator 22, thus entering the data into the next available RAM address."

This portion of Frankel et al describes transfer out of input data register 10 when it is full. However, this transfer disclosed in Frankel et al is not to the second buffer as recited claims 1 and 11. Note that both claims 1 and 11 recite that the second buffer outputs data at the second clock rate. Frankel et al includes no disclosure of the clock rate of his RAM input register 18. The Applicant submits that review of Frankel et al would make obvious operating RAM input register 18 at the input clock rate but not at the output clock rate as required by the recitations of claims 1 and 11.

Nor can RAM input register 18 or some combination of input data register 10 and RAM input register 18 be the first buffer recited in claims 1 and 11. Neither above quoted portions of Frankel et al include any teaching that RAM input register 18 is full or substantially full when data is copied the second buffer as

recited in claims 1 and 11. Further, RAM 16 does not operate at the second clock rate as recited in claims 1 and 11. Frankel et al states at column 3, lines 43 to 47:

> "The write/read sequence generator 22 repetitively produces the series of signals needed to write into the RAM 16 or read from it, and to control the address counters 16a. These signals are asynchronous with the buffer input and output clock rates."

This recitation of Frankel et al makes clear that RAM 16 does not operate at the second clock rate are recited in claims 1 and 11.

Kaneko also fails to make obvious this subject matter recited in claims 1 and 11. Kaneko includes no teaching that his first buffer memory copies data to the second buffer "when substantially full" as recited in claims 1 and 11. Kaneko includes numerous statements that data is transferred from his first buffer memory means to the second buffer memory means including: column 2, lines 34 to 36; column 2, lines 41 to 44; column 2, lines 63 to 65; column 3, lines 54 to 55; column 6, lines 27 to 28; column 7, lines 8 to 10; column 7, lines 13 and 14; column 8, lines 55 and 56; column 10, lines 24 to 27; column 10, lines 43 to 46; and column 10, lines 67 to column 11, line 3. Despite these numerous indications of data transfer from the first buffer memory means 21 to second buffer memory means 29, Kaneko fails to teach data copying from the first buffer to the second buffer takes place when the first buffer is substantially full. Kaneko teaches a full flag at column 8, lines 28 to 30, column 8, lines 58 or 65; column 9, lines 7 to 11; column 10, lines 16 to 18; column 11, lines 4 and 5; and column 11, lines 9 to 11. Note that all these references to a full flag are regarding second buffer memory means 29 and not first buffer memory means 21 as recited in claims 1 and 11.

The combination of Frankel et al and Kaneko teach transfer of data into the first buffer, out of the first buffer into the second

buffer and out of the second buffer to RAM. However, the references include no teaching that the data transfer from the first buffer to the second buffer takes place "when said first buffer is substantially full." Accordingly, the combination of Frankel et al and Kaneko fail to make obvious this recitation of claims 1 and 11.

Claims 1 and 11 recite further subject matter not made obvious by the combination of Frankel et al and Kaneko. Claim 1 recites a copy/access controller "operable to prompt said second component to access said second buffer when said data is copied from said first buffer." Claim 11 similarly recites the step of "prompting said second component to access said data in said second buffer when said copying step is completed." These limitations define when the second component accesses the data stored in the second buffer. These limitations are not made obvious by the combination of Frankel et al and Kaneko.

Kaneko includes no teaching regarding the timing and control of data movement between first buffer 21 and second buffer 29. The FINAL REJECTION cites Kaneko column 2, lines 42 to 53 as making obvious this limitation. Kaneko states at column 2, lines 38 to 53:

> "buffer checking/controlling means (300) for checking whether a storage condition of the second buffer memory means (29) corresponds to an empty state, thereby setting an empty flag when the storage condition becomes empty. The buffer checking/controlling means is also used for controlling transfer operations for the series of data from the first buffer memory means (21) to the second buffer memory means (29) and from the second buffer memory means (29) to the second storage means (1) of the computer (100) in such a manner that if, after the series of data read out from the first storage unit (5) has been transferred via the first and second buffer memory means (21:29) to the second storage unit (1), the empty flag is not yet set, an abnormal data transfer signal is issued. This prevents destructive read out of the data from the first storage unit (5)."

This portion of Kaneko teaches that the data stored in second buffer 29 is controlled to be transferred to the second storage unit 1. This portion of Kaneko fails to teach the event which triggers the second storage unit to access data stored in the second buffer 29. Kaneko teaches empty and full flags for second buffer 29. The transfer from second buffer 29 to second storage unit 1 could be triggered by the full flag of second buffer 29 indicating buffer full. This is a different event than recited in claims 1 and 11. The transfer from second buffer 29 to second storage unit 1 could be triggered by the empty flag of second buffer 29 indicating not empty. This is also a different event than recited in claims 1 and 11.

Note that claims 1 and 11 both recite prompting the second component to access data stored in the second buffer. Kaneko includes no indication that his second storage unit accesses data in the manner claimed.

Even if copying data from the first buffer to the second buffer eventually causes the later events disclosed in Kaneko (full flag indicating full or empty flag indicating not empty), this does not make obvious the prompt on copy to the second buffer recited in claim 1 and 11. The copying from the first buffer to the second buffer recited in claims 1 and 11 occurs at an earlier time than either Kaneko's full flag indicating full or Kaneko's empty flag indicating not empty. Thus these events of Kaneko are not the same event as recited in claims 1 and 11. The FINAL REJECTION fails to point out where Kaneko teaches the event triggering data transfer from the second buffer 29 to the second storage unit 1. The Applicant cannot find any such teachings. Thus Kaneko fails to make obvious this recitation of claims 1 and 11. The FINAL REJECTION does not point out any portion of Frankel et al as making obvious this limitation. Accordingly, claims 1 and 11 are allowable over the combination of Frankel et al and Kaneko.

The ADVISORY ACTION of January 23, 2004 in this application states "Applicant arguments made in view of the Kaneko reference are not well founded. The Kaneko reference teaches the second buffer, for temporary storing data to be transferred to a second component, after checking for data coincidence." The Applicant does not dispute that Kaneko teaches transfer of data from and external storage unit to a first buffer to a second buffer and hence to a host unit. The Applicant respectfully submits that the combination of Frankel et al and Kaneko fails to make obvious the particularly recited triggering events of claims 1 and 11. The first event when the first buffer is substantially full triggers copying to the second buffer. The second event when the data is copied to the second buffer triggers the second component accessing this data in the second buffer. It is these features that are not made obvious in the combination of Frankel et al and Kaneko.

Claims 2 to 4 and 12 to 14 are allowable by dependence upon respective allowable base claims 1 and 11.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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APPENDIX

CLAIMS ON APPEAL

1. A circuit for interfacing between a first component operating at a first clock rate and a second component operating at a second clock rate wherein said second clock rate is higher than said first clock rate, said circuit comprising:

a first buffer coupled to said first component, said first buffer receiving and storing data received from said first component at said first clock rate;

a second buffer coupled to said second component, said second buffer supplying data recalled therefrom to said second component at said second clock rate;

a copy/access controller connected to said first buffer, said second buffer, and said second component and operable to copy data from said first buffer to said second buffer when said first buffer is substantially full, and further operable to prompt said second component to access said second buffer when said data is copied from said first buffer.

2. The circuit as set forth in Claim 1, wherein both said first buffer and said second buffer are random-access memories.

3. The circuit as set forth in Claim 1, wherein both said first buffer and said second buffer are shift registers.

4. The circuit as set forth in Claim 1, wherein said circuit is integrated onto a semiconductor die with one of said first component or said second component.

11. A method for interfacing between a first component operable at a first clock rate and a second component operable at a second clock rate wherein said second clock rate is higher than said first clock rate, comprising the steps of:

transferring data from said first component to a first buffer operable at said first clock rate;

copying data from said first buffer to a second buffer operable at said second clock rate when said first buffer is substantially full;

prompting said second component to access said data in said second buffer at said second clock rate when said copying step is completed.

12. The method as set forth in Claim 11, wherein both said first buffer and said second buffer are shift-register structures.

13. The method as set forth in Claim 11, wherein both said first buffer and said second buffer are random access memories.

14. The method as set forth in Claim 11, wherein said first buffer and said second buffer are both integrated onto the same semiconductor die as one of said first component or said second component.